High Sensitivity InP-Based Monolithically Integrated pin-HEMT Receiver-OEIC's for 10 Gb/s

Wolfgang Kuebart, Jan-Hinnerk Reemtsma, Detlef Kaiser, *Member, IEEE*, Holger Grosskopf, Franziska Besca, Gerhard Luz, Wolfgang Körber, and Imre Gyuro

***Abstract*—InP-based pin-HEMT receiver-OEIC's with different circuit layouts for bit rates up to 10 Gb/s are simulated, realized and characterized. The circuits under investigation are a high impedance amplifier, a common-gate circuit, and a transimpedance-cascode circuit. The high frequency behavior of all circuits is compared by means of on wafer-characterization. All circuits show a bandwidth of more than 5 GHz, the transimpedance circuit has the highest responsivity (12.9 dB A/W) and a very low average noise current of 11.5 pA/$\sqrt{\text{Hz}}$ when assembled in a module. The receiver sensitivity of the transimpedance circuit in the module is measured to be as high as −19.2 dBm.**

I. Introduction

THE INCREASING number of advanced transmission systems leads to an increased demand for high speed ($\geq$10 Gb/s) photodetectors. There are a couple of different solutions for optoelectronic receivers under discussion. The key issue is the (pre-)amplification of the signal or bit-stream with low additional noise. The amplification can be done optically by an erbium-doped fiber amplifier (EDFA) or a semiconductor optical amplifier (SOA) [1]. An other approach is to amplify the signal within the photodetector by means of an avalanche photodiode (APD) (e.g. [2], [3]). Electronic amplification of the electrical output of the detector can be done e.g. by amplifiers based on silicon [4] preferably with a flip-chip bonded InP-based pin-diode or InP-electronics monolithically integrated with a pin-diode.

In this paper we focus on monolithically integrated optoelectronic receivers on InP. The most promising approaches include the pin-diode as a photodetector and either a heterojunction bipolar transistor (HBT) [5] or a high electron mobility transistor (HEMT) (e.g. [6], [7]) as amplifying devices. We prefer the latter one, because of its excellent noise properties [8].

II. Device Fabrication

The main goal is to achieve compatibility of the fabrication process for the pin-diode as a photonic device with the monolithic microwave integrated circuit (MMIC) technologies needed for the realization of the electronic HEMT-amplifier (Fig. 1). With respect to the quantum efficiency of the detector the absorption layer has a minimum layer thickness of 2 μm and the lateral dimensions are typically tens of microns. On the other hand the HEMT-layer sequence has a total layer thickness of only fractions of one micron. In addition the HEMT has lateral dimensions of one micron or even below thus requiring a planar surface for the optical lithography. The technological realization is based on a two step epitaxy on structured substrates similiar to [9], [10], leading to a quasi-planar alignment of the surfaces of HEMT and photodiode.

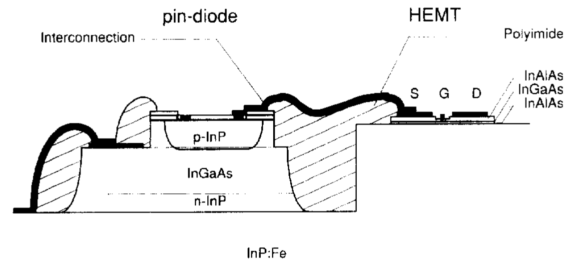


Fig. 1. Schematical cross section of a pin-HEMT receiver-OEIC monolithically integrated on InP.

The process starts with the growth of the HEMT layers by low pressure metal-organic vapor phase epitaxy (LP-MOVPE). Special attention was paid to the reduction of the oxygen background concentration by optimizing all growth parameters as e.g. temperature, pressure and III–V-ratio. By varying the III–V-ratio the oxygen concentration changes for more than two orders of magnitude. The lowest value we achieved is $1 - 2 * 10^{17}$ cm^{-3} measured by secondary ion mass spectroscopy (SIMS). Values measured with the same SIMS-equipment on commercially available wafers, which were grown either by molecular beam epitaxy (three suppliers) or MOVPE (one supplier), are in the same order of magnitude or higher. The layer sequence for the HEMT's consists of a 10 nm undoped InGaAs cap layer, a 20 nm undoped InAlAs Schottky barrier layer, a 15 nm n-doped InAlAs dopant layer ($N_D = 2.8 * 10^{18}$cm^{-3}), a 3 nm undoped InAlAs spacer, a 30 nm undoped InGaAs channel, and an undoped InAlAs/InP buffer on semi-insulating InP. Typical mobilities in the two-dimensional electron gas (2DEG) are ~10 000 and ~40 000 cm^2/Vs at 300 and 77 K, respectively.

After etching of recesses into the HEMT-layers and into the substrate the pin-layers are grown by LP-MOVPE , also (Fig. 1, see [11] for more details). The depth of the recesses has to be adjusted to the thickness of the pin-layer stack.

Manuscript received January 12, 1995; revised April 12, 1995. This work was supported in part by Deutsche Bundespost Telekom.

The authors are with the Alcatel SEL Research Centre, D-70435 Stuttgart, Germany.

IEEE Log Number 9413676.

0018–9480/95$04.00 © 1995 IEEE

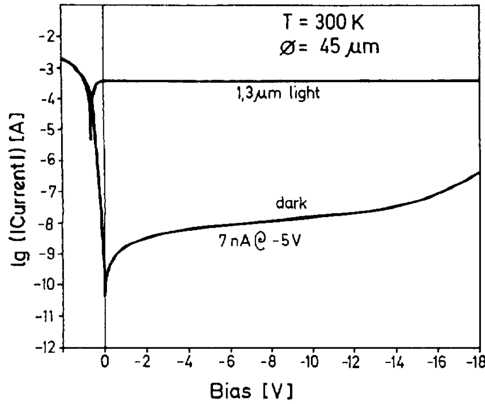


Fig. 2. Dark and photo current of a pin-diode with 45 μm diameter.

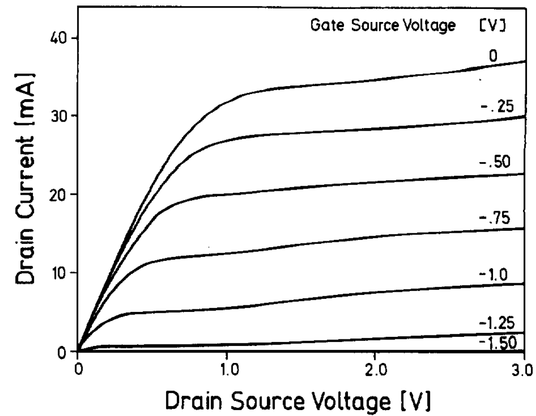


Fig. 3. Output characteristic of a discrete HEMT on an OEIC wafer with a gate of 1 * 100 μm^2.

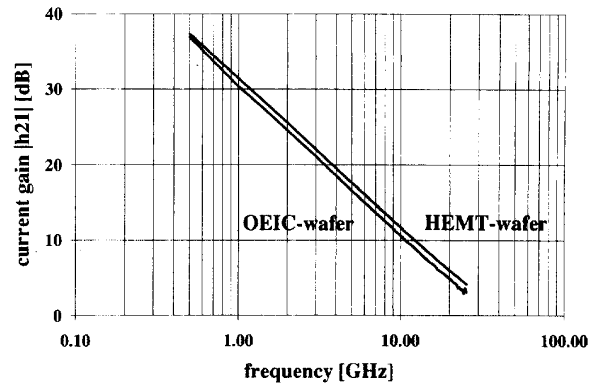


Fig. 4. Comparison of the short circuit current gain h_{21} of a discrete HEMT on an OEIC wafer and on single processed HEMT-wafers with same dimensiones ($l_g = 1\ \mu$m, $W_g = 100\ \mu$m) and bias points.

Typical background doping levels at 300 and 77 K in InP and InGaAs are $<5 * 10^{14}$ cm^{-3} and $<10^{15}$ cm^{-3}, respectively, while the mobilities exceed 200 000 and 90 000 cm^2/Vs at 77 K. The layer structure for the front illuminated pin-diode consists of an n^--doped InP cap layer, an undoped ternary absorption layer, and an n^+-doped InP layer. Zn- or Cd-diffusion with SiO_2 as a diffusion mask is used to define the p^+-region.

The detector layers are etched outside the pin-area to open the HEMT layers. AuZn/Ti/Pt/Au-based p-contacts are deposited directly on the p-diffused area, while the n-contacts (AuSn/Ti/Pt/Au) are formed on the ternary absorption layer. Both contacts are alloyed in one step using rapid thermal annealing (RTA), typical specific contact resistances are in the range of $10^{-5}\,\Omega$ cm^2 for the p-contact and $10^{-4}\,\Omega$ cm^2 for the n-contact. A mesa is etched outside the n-contacts down to the semi-insulating substrate in order to minimize parasitic pad and metallization capacitances. The dark current of devices with 45 μm diameter and a 30 μm diameter optical window is about 10 nA (Fig. 2). The series resistance of the device is below 15 Ω and the capacitance at a reverse voltage of 5 V is about 200 fF.

HEMT's, resistors and level shifter diodes are fabricated simultanously using the HEMT-layers, metal-insulator-metal structures (MIM) are used as capacitors. The process sequence is as follows. First the mesa is etched down to the InP buffer layer using wet chemical etching, mesa side wall etching is done using a selective etchant [12]. Then the lower metallization for the MIM capacitors (Ti/Pt/Au/Ti) and the ohmic contacts (AuSn/Ti/Pt/Au) for the HEMT's, resistors and level shifter diodes are deposited and alloyed by RTA. Typical contact resistances are below 0.5 Ω mm. SiO_2 is used as dielectricum for the capacitors. In order to reduce the number of process steps this layer is used as antireflective coating for the pin-diode, too. Gate lithography is performed optically to realize the 1 μm gates and the Schottky-contacts for the level shifter diodes, gate recess is done in a two step wet chemical etch process using a combination of selective and non-selective etchants. Gate metallization is Ti/Pt/Au. Polyimide is used to insulate the second metallization and is structured by reactive ion etching to open the contact holes. The second metallization serves as top electrode of the MIM-capacitors, as connection between the devices, and as bondpad-metallization.

A typical output characteristic of a discrete monitor HEMT on OEIC-wafers with a gate-length of 1 μm is shown in Fig. 3, the extrinsic transconductance exceeds 300 mS/mm, the corresponding extrinsic transit frequency measured on-wafer is higher than 30 GHz. Despite the additional epitaxial process the integrated HEMT's show almost no degradation in the high frequency behavior compared to single devices on HEMT wafers (Fig. 4). Gate leakage current in the bias point with maximum transconductance is well below 10 μA. The insulation resistance of the capacitors is better than 500 kΩ at a total capacitance of 7 pF.

The circuit simulation is performed using HSPICE [13]. In order to overcome limitations by existing device simulators we have implemented a table model into HSPICE. The DC characteristic of the HEMT's is incorporated via a two-dimensional table of measured working points. The high frequency properties are simulated using a table of frequency-independent small signal equivalent circuit elements [14] for each dc working point, too. The noise behavior is described using an additional noise current source in the standard small

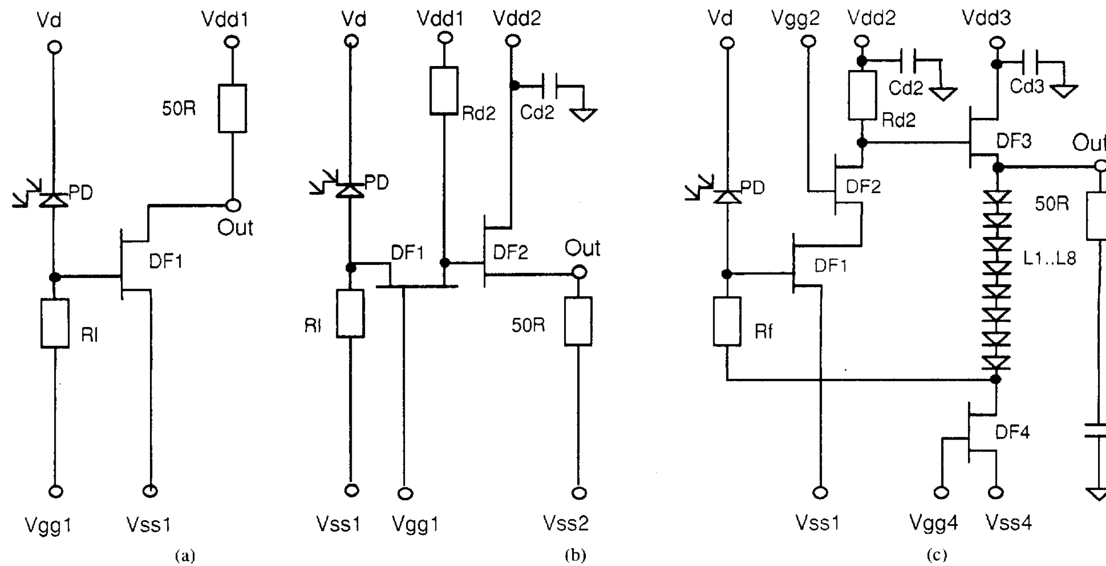


Fig. 5. Simplified circuit diagrams of three different realized receiver circuits: (a) high impedance common source OEIC (HI), (b) common-gate with source follower OEIC (GO), (c) transimpedance-cascode circuit with source follower OEIC (TI).

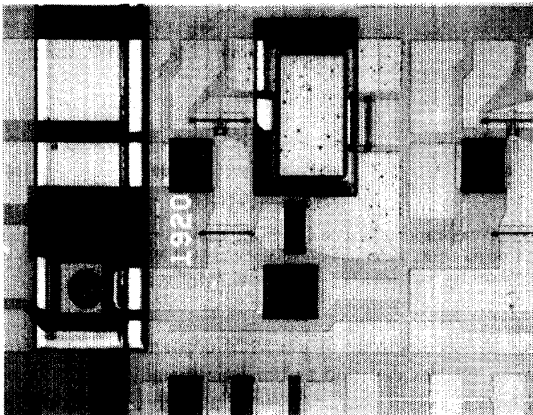


Fig. 6. Photograph of a realized common-gate pin-HEMT receiver-OEIC.

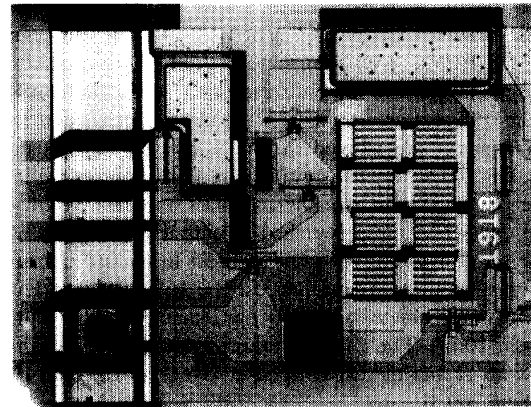


Fig. 7. Photograph of a realized transimpedance-cascode pin-HEMT receiver-OEIC with 21 devices.

signal equivalent circuit parallel to the channel equivalent circuit elements. Three different circuit concepts (Fig. 5) are simulated and realized afterwards (Figs. 6 and 7):

- single stage high impedance amplifier (named HI) with a load resistors of 60 Ω,
- common-gate input and source follower circuit (named GO),
- cascode input and source follower with transimpedance feedback and level shifter diodes (named TI).

The main results of the simulation are:

The high impedance circuit integrates only 3 devices, but it shows a rather high noise level ($\sim$24 pA/$\sqrt{\text{Hz}}$). The common-gate circuit appears to be a good compromise between noise performance ($\sim$15 pA/$\sqrt{\text{Hz}}$) and circuit complexity (8 devices). The transimpedance circuit has the lowest noise level ($\sim$9 pA/$\sqrt{\text{Hz}}$) and therefore the highest sensitivity, it combines 21 devices. The two latter circuits need on wafer blocking capacitors for critical DC-voltages to avoid instabilities.

III. On-Wafer Characterization

The high-frequency characteristics of these realized optoelectronic circuits are measured using on-wafer probing technique. A network analyzer modulates the 1300 nm calibrated laser source of a lightwave testset. A lightwave probe with a single-mode lensed fiber is used to illuminate the pin-photodiodes of the OEIC's. The diverse DC biases are provided to the circuits by coplanar multiple-power probe tips. A coplanar probe tip is used to detect the electrical response on-wafer. To characterize the optoelectronic devices

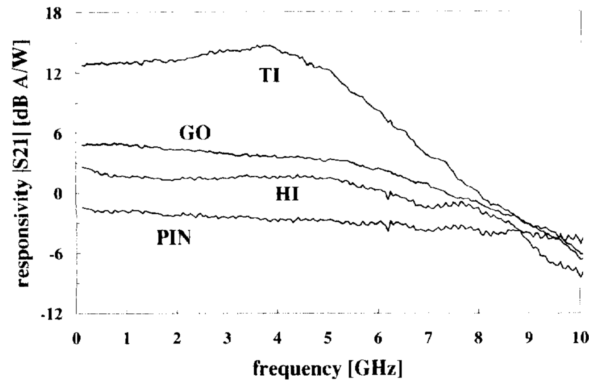


Fig. 8. On-wafer measured optoelectronic transfer functions of a discrete pin-photodiode (PIN) and three different types of receiver-OEIC's (HI, GO, and TI).

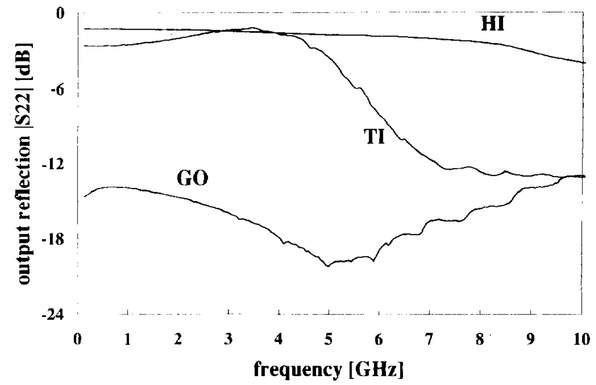


Fig. 9. On-wafer measured electrical output matching of the different types of receiver-OEIC's (HI, GO, and TI; cf. Fig. 8).

and circuits on-wafer as accurate as possible the simple response calibration of the lightwave testset is supplemented by a de-embedding procedure [15] to remove the attenuation effect of the non-insertable coplanar probe tip as well as reflective effects. In Fig. 8 the de-embedded optoelectronic transfer functions, i.e. the high frequency responsivity $|S_{21}|$ of the three different types of OEIC's and—in addition—of one discrete pin-photodiode are shown in the frequency range from 0–10 GHz. The absolute value of the responsivity is calibrated, too (0 db A/W means 1 A/W). The lowest trace (named **PIN**) belongs to the pin-photodiode and was measured at a reverse bias voltage of 5 V. A 3-dB bandwidth in the order of 10 GHz can be observed. From the lowest measured modulation frequency (130 MHz) a responsivity of -1.3 dB A/W (0.86 A/W) is determined. The other traces are transfer functions of the OEIC's. The high impedance circuit called **HI** reveals a fairly low responsivity of 2.8 dB A/W (1.38 A/W) due to the value $R_l = 60\ \Omega$ of the load resistor, which is necessary to achieve the observed bandwidth of 6.1 GHz. The small-signal response of the common-gate circuit **GO** with source follower can be seen in Fig. 8, too. The trace is very smooth without any reflective effects and reveals a 3 dB bandwidth of 6.8 GHz. The responsivity of 5 dB A/W (1.78 A/W) is slightly higher compared to the high impedance OEIC. The transimpedance-cascode circuit **TI** attains the highest responsivity of 12.9 dB A/W (4.41 A/W). Taking into account the responsivity of the pin-photodiode (-1.3 dB A/W) an electrical gain of 14.2 dB is found for the circuit in the 50 Ω system. This means, the transimpedance of the electrical part of the circuit is 260 Ω, which corresponds well to the value of the feedback resistor of 300 Ω. The trace shows a 3 dB-bandwidth of more than 5.5 GHz and no excessive peaking.

The measurement of the electrical output reflection S_{22} not only determines the quality of the output matching to the measurement system, but also gives evidence for possible instabilities. The magnitude of the electrical output reflection $|S_{22}|$ of all three OEIC's in the same operating point of Fig. 8 is depicted in Fig. 9. As can be observed, the high impedance circuit **HI** is highly reflective showing values in the order of only -1 dB for the magnitude of the output reflection. The transimpedance circuit **TI** is matched better. But transimpedance circuits with a peaking in their optoelectronic transfer function also exhibit a peaking in their electrical output reflection $|S_{22}|$. For circuits with too high internal loop gain (which can be achieved by variing e.g. the resistor R_{d2}, see Fig. 5), $|S_{22}| > 1$ is observed in the vicinity of the responsivity peak, which means, the circuit operates non-stable. The common-gate circuit **GO** using a source follower achieves a very good matching to the 50 Ω measurement system of better than -12 dB in the whole frequency range. This explains the very smooth transfer function without reflective effects observed for the GO circuit in Fig. 8.

The noise properties of the circuits are investigated on-wafer, too [16]. Without any optical input signal the output noise current is measured using a broadband low-noise amplifier (as the second amplification stage) and a spectrum analyzer. The equivalent input noise current density is calculated using the gain of the OEIC as the device under test (gain 1: cf. Fig. 8) as well as the second amplification stage (gain 2 $\approx$ 34.5 dB, noise figure NF 2 $\approx$ 2 dB). In Fig. 10 the equivalent input noise current densities of all three types of OEIC's of Fig. 8 are shown in the bandwidth of the devices. It is obvious, that the transimpedance-cascode circuit **TI** reveals the lowest equivalent input noise current density whereas the high impedance circuit **HI** with a load resistance of $R_l = 60\,\Omega$ shows the highest noise. The common-gate circuit with source follower **GO** indeed is a good compromise between noise performance and circuit complexity. Again, the trace of the common-gate circuit GO is clearly smoother than all other traces due to the good output matching of its source follower. The total medium noise current densities of all three OEIC's (HI, GO, and TI) up to 5 GHz are 31, 20, and 13.5 pA/$\sqrt{\text{Hz}}$, respectively. The transimpedance circuit shows values down to 11 pA/$\sqrt{\text{Hz}}$ in the frequency range of 1–2 GHz.

To demonstrate the capability for 10 Gb/s operation of the OEIC's a digital modulation experiment with the transimpedance circuit, which shows the best noise performance and therefore promises the highest receiver sensitivity, is performed on-wafer, too. A pattern generator modulates a 1.55-μm wavelength DFB-MQW-laser module (Alcatel SEL) with a 10 Gb/s nonreturn-to-zero (NRZ) pseudo-random bit

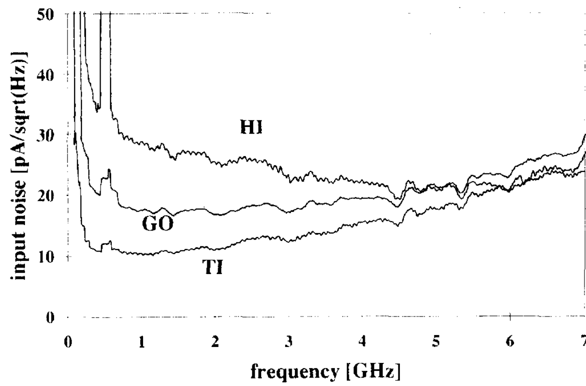


Fig. 10. On-wafer measured equivalent input noise current density of the different types of receiver-OEIC's (HI, GO, and TI; cf. Fig. 8).

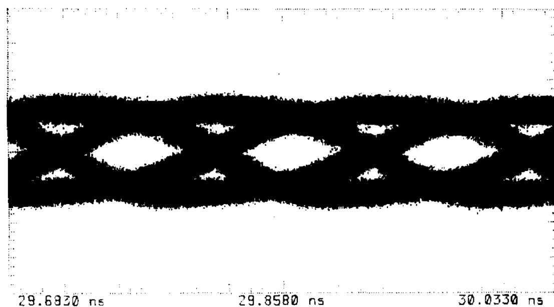


Fig. 11. On-wafer measured 10 Gb/s eye-diagram of a transimpedance-cascode circuit TI at an optical input power of −11.2 dBm (see text). Scale is 35 ps and 10 mV per division.

stream (PRBS). The extinction ratio is approximately 6.4 : 1, sequence length is $2^{23}-1$. Again the optical signal is coupled by the lensed-fiber to the OEIC and the electrical response is detected using a G-S-G wafer probe tip and analyzed by a sampling oscilloscope generating an eye-diagram. As can be seen in Fig. 11 the eye is clearly open at 10 Gb/s (persistance was infinite), which corresponds very well to the measured bandwidth. Optical input power is −11.2 dBm, lower power would have made post amplification necessary due to the sensitivity and noise level of the sampling oscilloscope.

IV. System Sensitivity of the Module

The transimpedance-cascode circuit **TI** is prepared for the investigation of the receiver sensitivity in a system transmission experiment. For that purpose chips are assembled into modules based on commercially available MMIC carriers. A mirror lens is used for fiber-chip coupling. With this flat module design, fiber and electronic feedthroughs lie in parallel to the electronic motherboard which facilitates very high speed operation at compact design. Fig. 12 shows the module with opened cover plate to allow a view on the block with the mirror lens.

To characterize the high speed and noise properties the transimpedance-cascode module **TI** is mounted into a microstrip test-bed with SMA-connectors to the electronic periphery. As can be seen in Fig. 13 there is no deterioration

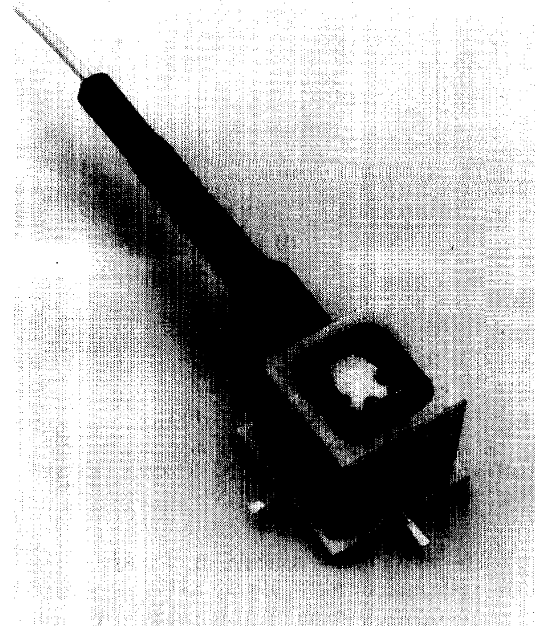


Fig. 12. Photograph of a transimpedance-cascode module.

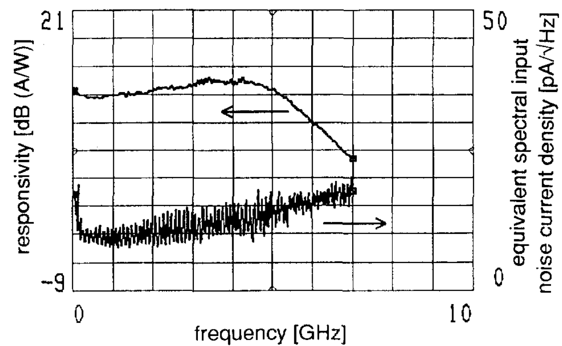


Fig. 13. Measured transfer function and equivalent input noise current density of a transimpedance-cascode module.

of the frequency response and the noise behavior observed after packaging compared to the on-wafer test. The 3-dB bandwidth is about 6 GHz, the frequency response is very flat with less than 2 dB peaking, and the responsivity at low frequencies is as high as 12.5 dB A/W (i.e.: 4.2 A/W). The equivalent input noise current density is shown in Fig. 13, too. At frequencies below 200 MHz the $1/f$ noise dominates, up to 4 GHz nearly white noise rises from only 8 pA/$\sqrt{\text{Hz}}$ up to 12 pA/$\sqrt{\text{Hz}}$, at higher frequencies the noise level slowly rises up to 17 pA/$\sqrt{\text{Hz}}$. The total average input noise current density in the bandwidth of the module is 11.5 pA/$\sqrt{\text{Hz}}$. This is the lowest value for 10 Gb/s monolithically integrated InP-based OEIC's reported up to now.

To determine the receiver sensitivity of the transimpedance-cascode module **TI** a 10 Gb/s system experiment is performed using the unshielded microstrip testbed. The optical output of a directly modulated 1.55 μm MQW-DFB-laser is fed into the connectorized fiber pigtail of the module. The electrical

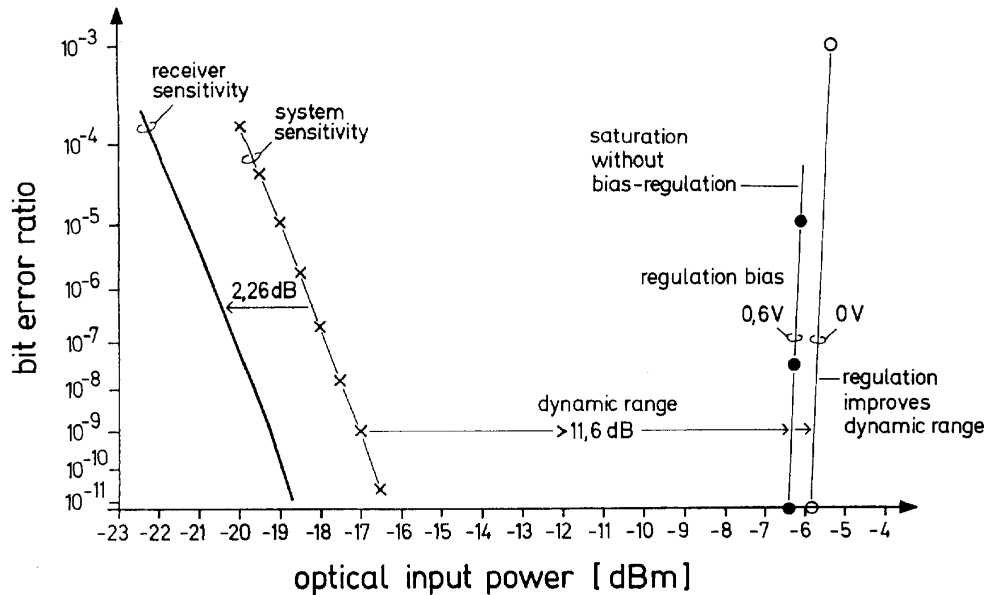


Fig. 14. Bit error ratio measurements at 10 Gb/s using a transimpedance-cascode module as receiver (see text).

output of the module is connected via the testbed and a DC-block capacitor to the input of a pre- and main-amplifier of the transmission system with clock recovery and decision circuit. A pattern generator is used to generate NRZ PRBS to perform the direct modulation of the laser. For a bit error ratio (BER) of 10^{-9} and a sequence length of $2^7 - 1$ a system sensitivity of -17 dBm is measured (see Fig. 14). This system sensitivity includes a penalty of 2.26 dB originating from the extinction ratio of the laser modulation, which is determined to be 3.9 : 1 using a simple "10"-pattern. Taking into account this penalty the receiver sensitivity is as good as -19.2 dBm, which is the highest sensitivity reported up to now for monolithically integrated 10 Gb/s pin-HEMT OEIC's. The dynamic range of the module is determined, too. As can be seen in Fig. 14, the bit error ratio is rapidly increasing when the optical input power exceeds approximately -6 dBm. This means that the dynamic range at a BER of 10^{-9} is at least 11.6 dB. By variation of one DC-bias of the transimpedance-cascode circuit it is possible to improve the dynamic range slightly.

V. Summary

We have simulated, realized and characterized three different pin-HEMT receiver-OEIC's. All circuits were measured on-wafer and show a 3 dB-bandwidth well above 5 GHz. The transimpedance-cascode circuit has the highest gain (12.9 dB (A/W)) and the lowest input noise level (13.5 pA/$\sqrt{\text{Hz}}$). The transimpedance-cascode circuit was mounted into a module without any degradation of the circuit performance in terms of gain, bandwidth and noise behavior; the input noise level is further reduced to an average value of 11.5 pA/$\sqrt{\text{Hz}}$. The receiver sensitivity of the module was measured to be -19.2 dBm at 10 Gb/s with a dynamic range of at least 11 dB.

Acknowledgment

The authors wish to thank K. Daub, K. Dütting, F. Grotjahn, G. Müller, L. Ovcar, J. Scherb, M. Ulmer, A. Volz, H. Conrad, and H. Gross for their excellent support.

References

[1] B. Mikkelsen, T. Durhuus, C. Joergensen. K. E. Stubkjaer, P. Doussiere, G. Garabedian, C. Graver, and D. Leclerc, "High performance semiconductor optical amplifiers as in-line- and pre-amplifiers," in *Proc. 20th ECOC 1994*, Fierenze, Italy, pp. 709–713.

[2] W. Kuebart, H. Eisele, J. Scherb, J. Kimmerle, P. Wiedemann, and W. Körber, "Continous graded 10 Gb/s planar InGaAs/InP SAGM-APD grown by LP-MOVPE," in *Proc. 17th ECOC & 8th IOOC 1991*, Paris, France, paper TuC5-2, pp. 253–256.

[3] I. Watanabe, S. Sugou, H. Ishikawa, T. Anan, K. Makita, M. Tsuji, and K. Taguchi, "Large gain-bandwidth-product, low current InAlAs/InAlGaAs quaternary-well superlattice avalanche photodiodes," *OFC/IOOC'93 Tech. Dig.*, paper ThG1, pp. 184–185.

[4] M. Neuhäuser, H.-M. Rein, H. Wernz, and A. Felder, "13 Gbit/s Si bipolar preamplifier for optical front ends," *Electron. Lett.*, vol. 29, pp. 492–493, 1993.

[5] L. M. Lunardi, S. Chandresekhar, A. H. Gnauck, C. A. Burrus, R. A. Hamm, J. W. Sulhoff, and J. L. Zyskind, "A 12 Gb/s high performance, high sensitivity monolithic pin/HBT photo-receiver module for long wavelength transmission systems," in *20th ECOC 1994*, Fierenze, Italy, post deadline papers, pp. 121–124.

[6] Y. Akatsu, Y. Miyagawa, Y. Miyamoto, Y. Kobayashi, and Y. Akahori, "A 10 Gb/s high sensitivity, monolithically integrated p-i-n-HEMT optical receiver," *IEEE Photon. Technol. Lett.*, vol. 5, pp. 163–165, 1993.

[7] W. Kuebart, D. Kaiser, H. Grosskopf, F. Besca, G. Luz, J.-H. Reemtsma, I. Gyuro, H. Conrad, H. Gross, and F. Grotjahn, "Monolithically integrated InP-Based PIN-HEMT receiver OEIC with a receiver sensitivity of -19.2 dbm at 10 Gbit/s," in *Proc. 20th ECOC 1994*, Fierenze, Italy, post deadline papers, pp. 79–82.

[8] P. Greiling, "InP-based microelectronics pilot line for commercial and military applications," in *Proc. 5th Conf. InP & Rel. Mat. 1993*, Paris, France, plenary paper, pp. 3–6.

[9] P. J. G. Dawe and D. A. H. Spear, W. S. Lee, G. R. Antell, and S. W. Bland, "Monolithic InP-based optical receiver front-end," in *Proc. 14th ECOC 1988*, post deadline papers, pp. 21–24.

[10] H. Nobuhara, H. Hamaguchi, T. Fujii, O. Aoki, M. Makiuchi, and O. Wada, "Monolithic pin HEMT receiver for long wavelength optical communications," *Electron. Lett.*, vol. 24, pp. 1246–1248, 1988.

[11] J.-H. Reemtsma, W. Kuebart, U. Koerner, J. Scherb, H. Eisele, K. Dütting, I. Gyuro, P. Wiedemann, F. Grotjahn, and J. Kimmerle, "Integrated high speed pin-diode grown by LP-MOVPE on selectively etched substrates," in *Proc. 3rd Conf. InP and Rel. Mat.*, Cardiff 8.-11.4.1991, Great Britain, paper MP.8, pp 114–117.
[12] S. R. Bhal and J. A. del Alamo, "Elimination of mesa-sidewall gate leakage in InAlAs/InGaAs heterostructures by selective sidewall recessing," *IEEE Electron. Dev. Lett.*, vol. 13, pp. 195–197, 1992.
[13] W. Kuebart, J.-H. Reemtsma, H. Gross kopf, I. Gyuro, D. Kaiser, H. Conrad, H. Gross , F. Grotjahn, and H. Eisele, "Monolithically integrated 10 Gbit/s InP-based receiver OEIC's: Design and realization," in *Proc. 19th ECOC*, Montreux, Switzerland, paper TuP6.4, pp. 305–308.
[14] B. Hughes and P. J. Tasker, "Bias dependence of the MODFET intrinsic model elements values at microwave frequencies," *IEEE Trans. Electron Dev.*, vol. 36, pp. 2267–2273, 1989.
[15] D. Kaiser, H. Grosskopf, F. Grotjahn, I. Gyuro, W. Kuebart, J.-H. Reemtsma, and H. Eisele, "De-embedding of on-wafer lightwave measurements performed on a monolithic 10 Gb/s InP receiver-OEIC," in *Proc. 23rd European Microwave Conf.. 1993*, Madrid, Spain, paper B 6.1, pp. 361–363.
[16] D. Kaiser, F. Besca, H. Grosskopf, I. Gyuro, J.-H. Reemtsma, and W. Kuebart, "Noise and small-signal performance of three different monolithic InP-based 10 Gb/s photoreceiver-OEIC's," *Electron. Lett.*, vol. 30, pp. 2070–2072, 1994.

Wolfgang Kuebart was born on March 29, 1951 in Göppingen-Holzheim, Germany. He received the Diploma degree in physics from the University of Stuttgart in 1978.

From 1978–1983 he worked as Research Assistant at the Physical Institute 4 of the University of Stuttgart (Prof. M. H. Pilkuhn). He established the work on physics and technology of GaAlSb/GaSb avalanche photodiodes and introduced the technology for InP/InGaAs photodiodes, especially the acceptor diffusion in InP. In 1983 he joined Alcatel SEL Research Center. He designed, realized, and characterized InGaAs/InP pin- and avalanche photodiodes. In 1989 the focal point of his work shifted to optoelectronic integrated receiver circuits for bitrates in the Gbit/s-range, where he became Head of the Processing Group for OEIC's. Currently he is responsible for the realization of the OEIC's. Semiconductor physics, device modelling, circuit design, plasma deposition and dry etching technologies, passivation and electrical characterization of the devices are the main fields of his work.

Mr. Kuebart is member of the Deutsche Physikalische Gesellschaft (DPG).

Jan-Hinnerk Reemtsma was born on April 16, 1960 in Düsseldorf, Germany. He received the Diploma degree in physics in 1985 from the Physical Institute 3 of the University of Düsseldorf, where he was working on CCD-cameras and investigations on metal-cyanid-complexes. In 1986 he joined the University of Duisburg (Prof. K. Heime), where he was engaged in the realization and characterization of p-channel HFET's. In 1989 he received the Ph.D. degree for his work.

That year he joined the Alcatel SEL Research-Center. Until 1994 he worked in the fields of InAlAs/InGaAs/InP OEIC's. The development of HEMT structures, design of mask sets, development of process schemes and realization of OEIC's were his main interests. Since the end of 1994 he has been engaged in the development of laser-modulator structures.

Dr. Reemtsma is member of the Deutsche Physikalische Gesellschaft (DPG).

Detlef Kaiser (M'91) was born 1958 in Castrop-Rauxel, Germany. He received the Dipl.-Phys. and the Dr. rer. nat. degrees in physics from the Westfälische Wilhelms-Universität Münster, in 1984 and 1990, respectively.

From 1984–1990, he worked as a Research Assistant at the Institut für Angewandte Physik of the WWU Münster, where he investigated Schottky-contact coplanar transmission lines on GaAs as voltage and optically controlled variable phase-shifter elements for MMIC's and OEIC's. In 1990, he joined the Opto-Electronic Components Division of the Alcatel SEL Research Center, Stuttgart, Germany, where he is currently engaged in the design and high-frequency characterization of all kinds of InP-based photodetectors and lasers. His main research interests include network analysis, de-embedding, digital transmission experiments and the on-wafer characterization of electronic and opto-electronic components and circuits.

Dr. Kaiser is a member of the Deutsche Physikalische Gesellschaft (DPG).

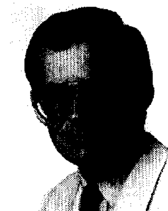
Holger Grosskopf was born on May 17, 1958 in Ulm, Germany. He received the diploma in electrical engineering in 1986 from the University of Stuttgart, where he was working on infrared black radiation sources.

In 1986 he joined the Alcatel SEL Research Center and worked first in the field of the realization of InGaAs/InP pin-JFET OEIC's, since 1990 in the realization of InGaAs/InAlAs/InP pin-HEMT OEIC's. His main interests are the installation of test equipment for process characterization, development of process steps and the realization of OEIC's.

Mr. Grosskopf is member of the Verband Deutscher Elektrotechniker (VDE).

Franziska Besca was born on January 6, 1967 in Mediasch, Roumania. She received the degree as Chemical Technical Assistant from the Chemical Institute Dr. Flad in Stuttgart in 1990.

Since 1990 she has been working as Research Assistant in the development of process steps and the processing and process characterization of optoelectronic integrated circuits.



Gerhard Luz was born on June 28, 1953 in Neuhausen ob Eck, Germany. He received the diploma in physics in 1979 from the University of Stuttgart, where he was working on optical gain in III–V laser materials.

In 1979 he joined the Alcatel SEL Research-Center. His work covered the optoelectronic characterization of lasers and photodetectors. In 1986 he became Head of the group for Optoelectronic Packaging. His main working fields are the design, modeling and realization of packages for optoelectronic components for transmission rates in the Gb/s-range.

Wolfgang Körber was born in Stuttgart, Germany on July 10, 1956. He received the diploma and Ph.D. degree in physics from the University of Stuttgart in 1982 and 1988, respectively. The Ph.D. work dealt with "Epitaxial Incorporation and Optical Properties of Rare Earths in III–V-Semiconductors."

In 1988 he joined the Alcatel SEL Research Center where he first was in charge with LPE-growth of PIN and APD Detector Structures. Since 1992 he has been responsible for MOVPE of detector and HEMT structures and also for receiver OEIC regrowth techniques.

Dr. Körber is member of the German Association of Crystal Growth DGKK.

Imre Gyuro was born on November 12, 1953 in Nyirbeltek, Hungary. He received the diploma in electronics engineering in 1978 from the Technical University of Budapest, Hungary, where he was working on VPE growth of GaAs based structures. In 1978 he joined the Institute for Technical Physics of the Hungarian Academy of Sciences, where he was engaged in the VPE growth of GaAs based layer structures for microwave applications (Gunn-, Schottky diodes and MESFETs). In 1986 he received the Ph.D. degree. His thesis covered the bulk crystal growth of III–V materials under microgravity conditions. In 1988 he received a research fellowship from the Alexander von Humbold Foundation and spent 18 months at the University Duisburg (Prof. K. Heime) where he was involved in the MOVPE growth of AlGaAs/GaAs layer structures and in the development of HIGFET transistors.

In March 1990 he joined the Alcatel SEL Research Center where he was engaged in the MOVPE growth of InP-based materials for optoelectronic applications. In 1992 he became responsible for detector epitaxy and since 1993 he has been Manager of the Epitaxy Group at the Opto-Electronics Division.